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ECPE 174

**Progress Report #1 & #2**

November 20th:

I explored ideas of how to make the stopwatch portion of the project function. The first step, and in my mind easiest, was to change the clock divider. The clock divider is originally set to break down a 27 MHz clock down to 1 Hz. However, the stopwatch not only counts seconds, but down to hundredths of seconds. Therefore, the stop watch would need to have a clock divider that limited the system to 100 Hz. In VHDL, this meant setting the clock divider to count every 135,000 positive clock edges, rather than 13,500,000 positive clock edges. The biggest challenge was to understand how to make all 7 segment displays output one variable. I did not land on an idea that would allow me to do this, and decided I would figure out an idea by next week.

November 27th:

I came to a conclusion of how to represent one variable on all four 7 segment displays. However, the 7 segment displays technically output four variables. I decided to make the stopwatch behave as an enormous counter, as each 7 segment display would represent an individual counter. The hundredths of a second counter would go from 0 to 9, then back to 0. Once the hundredths of a second counter reached the end of the FSM, an overflow of “1” would be registered. Once this overflow is registered to the system, the tenths of a second would move from 0 to 1, then wait for another overflow of “1” to register until it incremented. All four 7 segments would be conducted on a constant stream of overflows, in which case the 7 segment displays would resemble a stopwatch. However, the code itself is not completed, therefore this is what I will be working on this upcoming week.